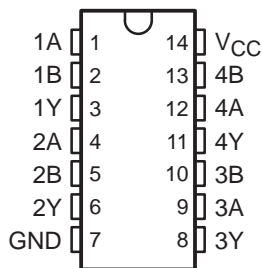


SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

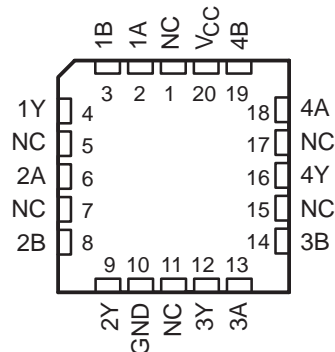
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 10$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- True Logic

SN54HC86 . . . J OR W PACKAGE
SN74HC86 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC86N	SN74HC86N
	SOIC – D	Tube of 50	SN74HC86D	HC86
		Reel of 2500	SN74HC86DR	
		Reel of 250	SN74HC86DT	
	SOP – NS	Reel of 2000	SN74HC86NSR	HC86
	TSSOP – PW	Tube of 90	SN74HC86PW	HC86
Reel of 2000		SN74HC86PWR		
Reel of 250		SN74HC86PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC86J	SNJ54HC86J
	CFP – W	Tube of 150	SNJ54HC86W	SNJ54HC86W
	LCCC – FK	Tube of 55	SNJ54HC86FK	SNJ54HC86FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

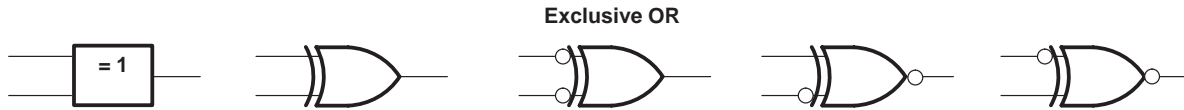
SCLS100E – DECEMBER 1982 – REVISED AUGUST 2003

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

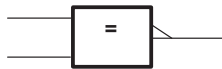
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

Logic Identity Element



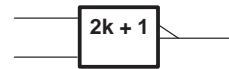
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

Even-Parity Element



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

Odd-Parity Element



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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recommended operating conditions (see Note 3)

		SN54HC86			SN74HC86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5	0.5	V	
		V _{CC} = 4.5 V			1.35	1.35		
		V _{CC} = 6 V			1.8	1.8		
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V			1000	1000	ns	
		V _{CC} = 4.5 V			500	500		
		V _{CC} = 6 V			400	400		
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC86		SN74HC86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9	1.9	V		
			4.5 V	4.4	4.499		4.4	4.4			
			6 V	5.9	5.999		5.9	5.9			
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7	3.84			
		I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2	5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1	0.1	V	
			4.5 V		0.001	0.1		0.1	0.1		
			6 V		0.001	0.1		0.1	0.1		
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4	0.33		
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4	0.33		
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000	±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			2		40	20	μA	
C _i			2 V to 6 V		3	10		10	10	pF	



SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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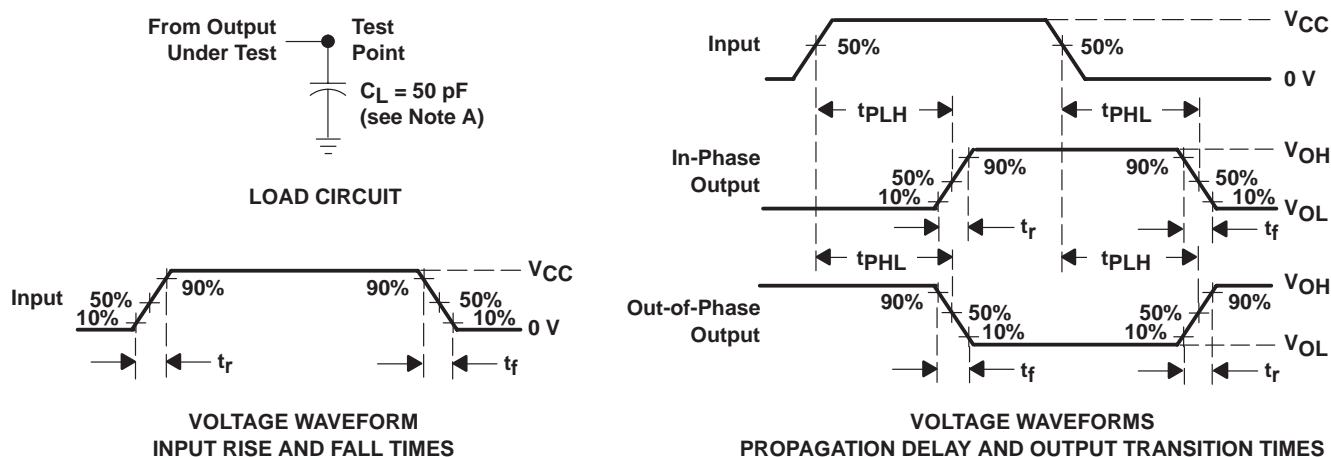
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC86		SN74HC86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84046012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84046012A SNJ54HC 86FK	Samples
8404601CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404601CA SNJ54HC86J	Samples
8404601DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404601DA SNJ54HC86W	Samples
JM38510/65202BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65202BCA	Samples
M38510/65202BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65202BCA	Samples
SN54HC86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC86J	Samples
SN74HC86D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC86N	Samples
SN74HC86NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC86N	Samples
SN74HC86NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC86NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SN74HC86PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC86	Samples
SNJ54HC86FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84046012A SNJ54HC 86FK	Samples
SNJ54HC86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404601CA SNJ54HC86J	Samples
SNJ54HC86W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404601DA SNJ54HC86W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC86, SN74HC86 :

- Catalog: [SN74HC86](#)
- Automotive: [SN74HC86-Q1](#), [SN74HC86-Q1](#)
- Military: [SN54HC86](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC86DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC86PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC86DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC86DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC86DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC86PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC86PWT	TSSOP	PW	14	250	367.0	367.0	35.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

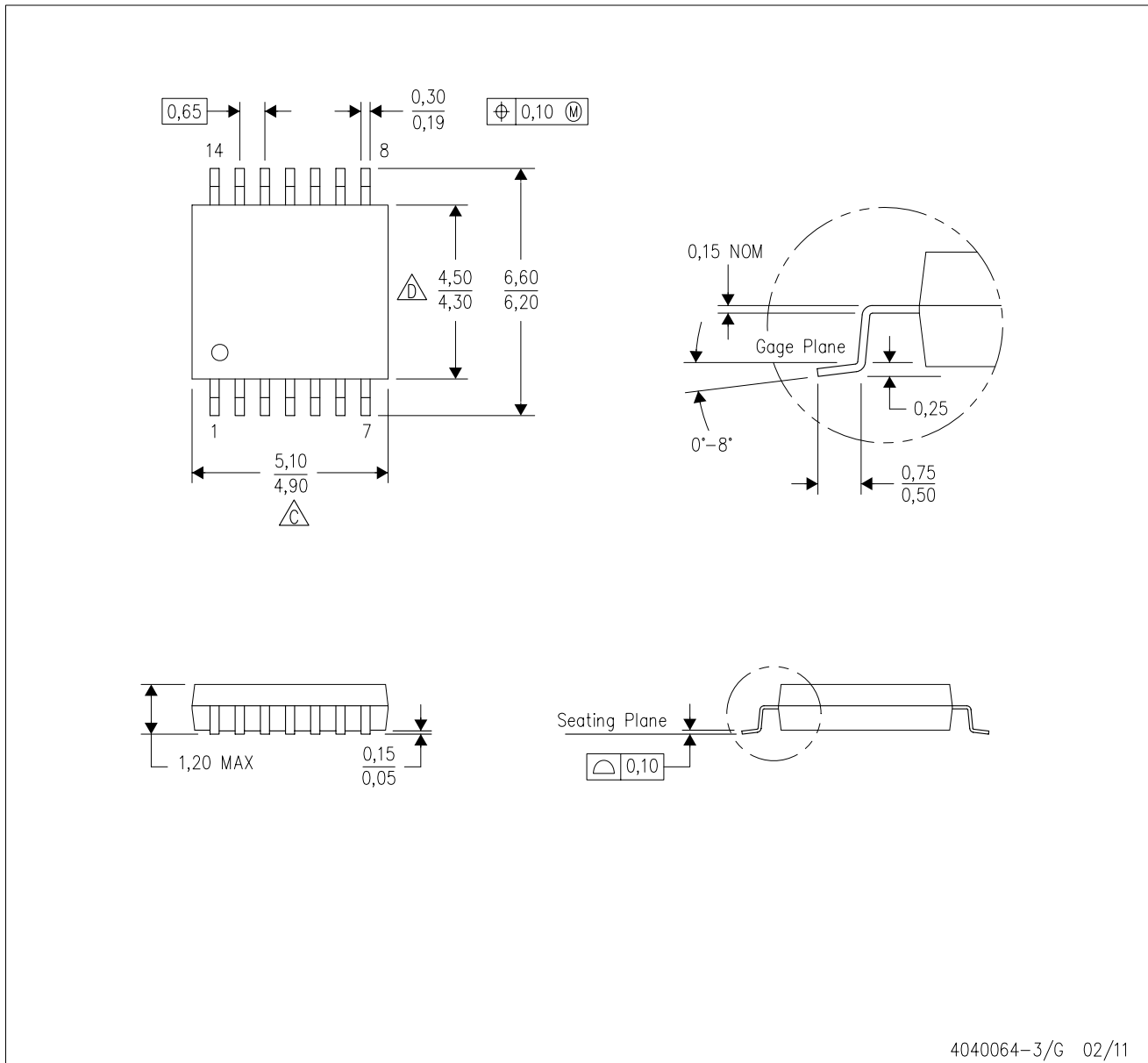


4211283-3/E 08/12



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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