ANUP KUMAR DAS

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Summary

I am an assistant professor at Drexel University. A life-long learner and an engineer by training, motivated to transform students to well-renowned computer engineers and scientists of the future, simultaneously driving research directions leading to breakthroughs and securing project grants, enabling neuromorphic center of excellence at the institute.

Education

2011 – 2014: Ph.D. in Computer Engineering (Embedded Systems)
National University of Singapore, Singapore

- Thesis: Design Methodologies for Reliable and Energy Efficient Multiprocessor Systems
- GPA: 3.83

2000 – 2004: B.E. in Electronics and Telecommunication Engineering
Jadavpur University, India

- Thesis: Analysis of Blocking Probability for Optical WDM Networks
- GPA: 3.89

Work Experience

ASSISTANT PROFESSOR – DREXEL UNIVERSITY

Philadelphia, PA
Jan'18 – Present

Leading the computer architecture research at Drexel University with focus on neuromorphic computing using non-volatile memories. Currently teaching the following courses.

- ECEC 621: High Performance Computer Architecture (Winter'18, Fall'18)
- ECEC 623: Memory Architecture (Advanced Computer Architecture) (Spring'18)

RESEARCHER – IMEC

Eindhoven, Netherlands
Nov'15 – July'17

- Mining of real-time ECG time-series data for unsupervised heart-rate estimation.
- Finger- and wrist-PPG-based heart-rate estimation using deep learning.
- Autonomous guidance of helium balloon using deep reinforcement learning.
- Sensor fusion for air quality monitoring using spiking neural network.
- Mapping of LTE-A PHY processing on microserver using reinforcement learning.

RESEARCH FELLOW – UNIVERSITY OF SOUTHAMPTON

Southampton, United Kingdom
June'14 – Oct'15

- Thermal and power modeling for many-core systems using multinomial logistic regression.
- Run-time thermal management of many-core embedded systems using reinforcement learning.
- Control theory-based voltage adaptation for power-neutral IoT nodes.

RESEARCH SCHOLAR – NATIONAL UNIVERSITY OF SINGAPORE

Singapore
July'11 – May'14

- Data-flow based mapping of multimedia applications on multiprocessor systems.
- Use of evolutionary techniques to optimize reliability of multiprocessor systems.
- Reinforcement learning based power-performance trade-off on embedded systems.

SENIOR DESIGN ENGINEER – LSI CORPORATION (NOW BROADCOM) Bangalore, India
Jan'08 – July'11

- Frontend design of maximum a posteriori probability (MAP) decoder for read channel of Solid-State Drive (SSD) SoC.
- Low power design for test (DFT) of multi-power domain SSD SoC.

MEMBER OF TECHNICAL STAFF – TRANSWITCH CORPORATION New Delhi, India
Aug'07 – Jan'08

- RTL designer for ethernet packet processor.

DESIGN ENGINEER II – STMICROELECTRONICS Greater Noida, India
July'04 – Aug'07

- Frontend design of Audio Peripheral IPs such as PCM Player, SPDIF Player and 5.1 channel DTS.
- Frontend design of HDMI and HDCP.

Soft Skills

Python (numpy, scipy, scikit-learn, caffe, theano, brian2)
R, C++, C#, Matlab, Perl, TCL, Shell
Operating Systems (Linux, Mac OS, Windows)
Subversions (SVN, Git)
Cloud Technology (Google Cloud and AWS)

Quantifiable Results

Co-PI: EDL: Efficient Deep Learning (Sub-project: Low power hardware for neural networks)

- STW-NL, 64K Euros

Co-PI: MNEMOSENE: Computation-in-memory architecture based on resistive devices

- EU-H2020, 6.4M Euros

Co-PI: PARTNER: Patient-care Advancement with Responsive Technologies and Engagement Together

- ITEA3, 128K Euros

Co-PI: NeuRAM3: Neural Computing Architectures in Advanced Monolithic 3D-VLSI Nano-technologies

- EU H2020, 4.8M Euros

Administrative Duties

Currently Serving Technical Program Committee: ICCD (2018), FPL (since 2013), DATE (since 2017), DAC (since 2017), CASES (since 2017), GLSVLSI (2018), IGSC (since 2017)
Organizing Committee: Vice Chair SIGDA University Demonstration 2018, Publicity Chair, SIGDA University Demonstration 2017
Regular Reviewer: IEEE TCAD, IEEE TVLSI, IEEE TC

Honors

- 2004: Gold Medal for highest performance in the batch of 2004 at Jadavpur University
- 2004: Recognition for contribution to the design of Set Top Box integrated circuits at ST Microelectronics
- 2007: Best paper award at LSI Annual Technical Conference on best DFT practice of multi-power domain SoC
- 2013: Singapore President's Fellowship for achievements in research and studies (top 10% of 1300 Phds)
- 2015: Best paper candidate at DATE conference 2015
- 2016: Best paper candidate at DATE conference 2016
- 2016: Three proposals accepted at IMEC -- 1 EU H2020, 1 ITEA3 and 1 Dutch STW on topics related to neuromorphic computing.
- 2017: 1 book and 2 book chapters published. Honored by Drexel University Library

- 2018: $2M proposal on neuromorphic computing submitted (currently under review) to NSF Smart and Connected Community as a PI, within 3 months of joining Drexel. Two more proposals are under preparation.

Publication Records

- US Patents: 1
- Book: 1
- Book Chapters: 3
- Peer Reviewed Journals: 15 (two under preparation)
- Peer Reviewed Conferences: 33 (four under review)