

# Custom VLSI Design & Analysis I

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ECE-C 572

Winter

Prof. Ioannis Savidis

Syllabus

Lec: 1h50m

Lab: 1h50m

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## Course Information

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Course Title: Custom VLSI Design & Analysis I  
Course Type: Undergraduate/Graduate cross listing (CRN: )  
Credits: 3 credits  
Duration: Winter Quarter

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## Instructor and TA Information

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Instructor: Prof. Ioannis Savidis  
Email: isavidis@coe.drexel.edu  
Office: Bossone 413J  
Teaching Assistant: Ms. Ying Teng  
Office: Bossone 324

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## Intended Audience

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This course is intended for **senior-level ECE undergraduate students** and **graduate students**. The workload for graduate and undergraduate students will differ, and the two groups will be evaluated independently.

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## Prerequisites

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Knowledge of VLSI design (**ECE-C 471/571**) is required. Previous exposure to transistors and semiconductor devices would be useful but not required.

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## Course Description

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This is the first of two courses offered on *Custom Very Large Scale Integration (VLSI) circuit and systems design and analysis*. An understanding of VLSI integrated circuits is achieved through circuit design and analysis. This course focuses exclusively on high performance digital CMOS VLSI circuit and systems design, although some topics on mixed-signal circuits are also addressed.

Design and analysis of VLSI integrated circuits will be covered from the circuits and systems design perspectives. First, a thorough analysis of interconnect networks is presented. Interconnect modeling and extraction is explored. Signal propagation analysis based on lumped and distributed models provides insight to both local and global signaling. Interconnect coupling noise is also analyzed and modeled. The second part of the class focuses on synchronization of high performance ICs. A focus on on-chip clock generation and distribution is provided. Synchronous system characteristics are also explored including analysis and modeling of different clock topologies, clock buffering, and clock skew scheduling.

Course topics include:

1. Interconnect modeling and extraction
2. Interconnect coupling noise
3. Signal propagation analysis
4. Global signaling
5. Synchronization theory
6. On-chip clock distribution
7. On-chip clock generation

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### Learning Goals

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By the end of the course, students will:

- Analyze the electrical impedance of the on-chip interconnect.
- Distinguish between the different electrical models of the interconnect, and determine under which conditions the models are valid and accurate.
- Analyze different sources of noise coupling including capacitive, inductive, and active and passive device noise.
- Describe design considerations and techniques for global signaling including repeater insertion, shielding, and gate sizing.
- Classify boolean signals as applied to circuit synchronization.
- Compare different circuit synchronization schemes, and understand the advantages and limitations of each.
- Examine and analyze different on-chip clock generation methods including ring oscillators, crystal oscillators, phase-locked loops, and delay-locked loops.
- Understand timing characteristics of the clock signal (setup and hold times, clock skew, etc.).
- Analyze and model the clock distribution network.
- Analyze the role of computer-aided design tools (SPICE and Cadence-Layout and simulation) in automating the design flow, resulting in increased productivity in VLSI systems design (focus on using design tools to properly design the clock network).
- Learn cooperative team building skills through homework and laboratories with the goal of applying design principles to minimize certain objective functions while meeting other design constraints for a functional circuit.

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## Course Structure

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- Laboratory: Once a week, multiple lab assignments.  
Exam(s): Two (2) exams, one midterm and a final examination.  
Homework(s): Two (2) homework assignments.  
Project(s): Two (2) projects.

This is a senior level undergraduate and graduate level class. The evaluation criteria is adjusted according to the academic level of the student. The evaluation process includes an analysis of the quality of individual work as well as participation in group projects (homework and lab) and lectures. The final grade will be calculated as follows:

|              |             |
|--------------|-------------|
| Final exam   | 30%         |
| Midterm exam | 15%         |
| Project(s)   | 45%         |
| Homework(s)  | 10%         |
| <i>Total</i> | <i>100%</i> |

A mix of individual and student paired homework will be assigned. Homework assignments must be submitted at the beginning of class on the day they are due. Homework submitted more than three days late will not be graded. Late homework is penalized 15% per day until the third day (days are considered at noon). All requests for a re-grade must be submitted in writing within a week of the assignment being returned. No assignment will be re-graded after one week. Please let me know immediately if I incorrectly added your score.

The midterm exam is a take-home exam. Student pairs will complete the midterm exam and submit a combined test booklet for scoring. The final exam is an *individual*, in-class exam tentatively scheduled for exam week. All exams must be taken at the scheduled time unless a previous arrangement (with a good reason) has been made with the instructor. Good reasons include medical conditions, family emergencies, and religious observation.

Note that this course is cross-listed as a graduate level course. Graduate and undergraduate course work *differs*, and students are evaluated *independently*. Graduate students are assigned more questions on the both homeworks and examinations.

The instructor and the TA will provide feedback on any assignment submitted on time within two weeks after the submission deadline. For late submissions, feedback will be provided within two weeks from the date of submission. For laboratory work that was started (and worked on) during laboratory hours, immediate feedback will be provided by the laboratory instructor (TA and/or instructor). There will be minimal to no feedback during the laboratory hours on laboratory assignments assigned during previous weeks. Feedback provided during laboratory sessions typically consists of corrections to student work and personal instruction. Feedback outside the laboratory hours typically includes a repeat of the instructions given during the laboratory session for the given laboratory assignment and resolving potential system errors (software problems, account problems, etc.), but not correction of errors in student work.

The Academic Policies set by the Drexel University Office of the Provost dictates the scale of letter grades as pertaining to grade point average (<http://www.drexel.edu/provost/policies/grades.asp>). The percentages used to assign these grades are listed below.

| Letter | Grade Percentage |
|--------|------------------|
| A+     | 97-100%          |
| A      | 93-96.9%         |
| A-     | 90-92.9%         |
| B+     | 87-89.9%         |
| B      | 83-86.9%         |
| B-     | 80-82.9%         |
| C+     | 77-79.9%         |
| C      | 73-76.9%         |
| C-     | 70-72.9%         |
| D+     | 67-69.9%         |
| D      | 63-66.9%         |
| F      | Below 63%        |

The instructor reserves the right to adjust the grade percentages (e.g. based on the distribution of grades) to accommodate non-standard (low or high) distributions.

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### Lectures

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Lecture is a time for individual and group learning. Distractions during class reduce the overall quality of academic growth. Cell phone use is therefore prohibited during lecture. All cell phones must be placed in silent mode. You should not be talking, web-surfing, or texting on your phone during class. If you need to use your phone in any way, please leave the classroom.

Laptops are permitted during lecture for the explicit use of note taking or searching for additional information on a topic of discussion. Laptop use in class is a privilege. If the use of your laptop becomes a distraction to other students, laptops will be banned from use.

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### Class Website

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We will use Drexel's **Blackboard Learn** course management website for this class. I will mail you important information regarding the class through this system. Please make sure you setup the system to forward BB/Learn emails to an account you check regularly. Homework, homework solutions, supplemental materials, etc. will be posted on the main course page.

If you want to email me or the TA, please do so at the email addresses listed above. This is preferred to emailing us from within Blackboard Learn.

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### Attendance Policy

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You are expected to attend each class punctually and remain for the entire class period. You need to inform the instructor in advance if you expect to miss a class or leave the course before the end of the semester. If you miss class your absence will be excused by the instructor only if a valid doctors certificate or other evidence is submitted. You remain responsible for the work associated with the class you missed, even if your absence has a valid reason.

A 5% reduction in a student's overall quarterly score will be assessed for every three days of unexcused absence. Please make sure to attend each class as a role call will be made at the beginning of each lecture period.

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## Class Withdrawal

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A student may withdraw from the course at any time during the term, but before the deadline established in the University Academic Calendar. A discussion with the instructor is advised before a withdrawal is undertaken.

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## Academic Dishonesty

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Cheating in any form is not tolerated, nor is assisting another person to cheat. The submission of any work by a student is taken as a guarantee that the thoughts and expressions in it are the students own except when properly credited to another. Violations of this principle include giving or receiving aid in an exam or where otherwise prohibited, fraud, plagiarism, the falsification or forgery of any record, and any other deceptive act in connection with academic work. Plagiarism is the representation of anothers words, ideas, programs, formulae, options or other products of work as ones own work from others, since it is often not possible to determine who the originator or the copier was. Such offense will result in a failing grade "F".

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## Textbook

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The required textbook and additional reference textbooks are listed below. The additional textbooks provide additional information on VLSI design and are quite useful.

**Required Textbook:** E. Salman and E. G. Friedman, *High Performance Intergrated Circuit Design*, McGraw-Hill Inc., 2012.

**Additional Textbooks:**

1. J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, Prentice Hall, 2<sup>nd</sup> edition, 2003.
2. N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley, 3<sup>rd</sup> ed., 2005.
3. R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, John Wiley & Sons, 3<sup>rd</sup> ed., 2011.
4. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, McGraw-Hill Inc., 3<sup>rd</sup> ed., 2003.
5. D. A. Hodges, H. G. Jackson, and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits In Deep Submicron Technology*, McGraw-Hill Inc., 3<sup>rd</sup> ed., 2004.
5. IEEE Transactions on VLSI.
6. IEEE Transactions on Computer-Aided Design.
7. IEEE Transactions on Circuits and Systems, Part II-Systems.
8. IEEE Transactions on Computers.

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## Laboratory/Projects

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Two quarter-long projects are assigned. One project (individual) is a literature search and paper on a topic related to high performance IC design in synchronization and interconnects. The second project (group) is the development of an integrated circuit implementing a group defined function (cosine transfer function, pipeline array multiplier, edge detection systems, high-speed 32-bit signed/unsigned pipelined multiplier, etc.). A focus on the clock distribution network and interconnect design is emphasized.

Laboratory sessions are used to address project objectives between group members. Weekly design meetings include group progress reports, discussion of design specifications, and discussion of problems in design. Cadence CAD tools are used throughout the quarter. Specifically, the Cadence Virtuoso toolset is used for schematic capture, simulation, layout, and pre- and post-layout analysis. Students will use the Cadence Analog Artist environment for circuit simulation and analysis, and Diva/Assura/Calibre for design rules checking (DRC) and layout versus schematic (LVS) verification of layouts.

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### Tentative Schedule

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| Week | Lecture                               | Chapter | Lab | Homework     |
|------|---------------------------------------|---------|-----|--------------|
| 1    | Introduction to custom VLSI design    | 1       |     |              |
| 2    | Interconnect scaling and enhancements | 2       |     |              |
| 3    | Interconnect modeling and extraction  | 3       |     | HW#1         |
| 4    | Signal propagation analysis           | 4       |     |              |
| 5    | Interconnect coupling noise           | 5       |     | Midterm Exam |
| 6    | Global signaling                      | 6       |     |              |
| 7    | Synchronization theory and tradeoffs  | 12      |     |              |
| 8    | On-chip clock generation              | 13      |     | HW#2         |
| 9    | Synchronous system characteristics    | 14      |     |              |
| 10   | On-chip clock distribution            | 15      |     |              |
| 11   | <b>Final Examination</b> (Date TBA)   |         |     |              |

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### Academic Policies

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The academic policies defined by the Office of the Provost are upheld for this course. The complete list of policies (academic and otherwise) are listed at <http://www.drexel.edu/policies>. Students should pay particular attention to the following policies:

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|---|---|
| Academic Integrity                      | <a href="http://www.drexel.edu/provost/policies/academic_dishonesty.asp">http://www.drexel.edu/provost/policies/academic_dishonesty.asp</a>                       |
| Course Drop Statement                   | <a href="http://www.drexel.edu/provost/policies/course_drop.asp">http://www.drexel.edu/provost/policies/course_drop.asp</a>                                       |
| Disability Statement                    | <a href="http://www.drexel.edu/oed/disabilityResources/Overview/">http://www.drexel.edu/oed/disabilityResources/Overview/</a>                                     |
| Student Conduct and Community Standards | <a href="http://www.drexel.edu/studentaffairs/community_standards/studentHandbook/">http://www.drexel.edu/studentaffairs/community_standards/studentHandbook/</a> |

**Course Change Policy:** The instructor reserves the right to change the course during the quarter at his discretion. All changes, if applicable, will be communicated to the students verbally during class or through Blackboard Learn Announcements. Every effort will be made to

1. Not change any course policy past the course withdrawal period.
2. Collect student feedback prior to implementing any course change.