ECEC690 ST:Network-on-a-Chip (NoC) I	Syllabus
Fall quarter	Lec: 2 lectures, 1h20m each
Prof. Baris Taskin	Lab: None

Course Information

Course Title:	Special Topics: Network-on-a-Chip (NoC) I
Course Type:	Graduate course
Credits:	3 credits

Instructor and TA Information

Instructor:	Prof. Baris Taskin (taskin@coe.drexel.edu)
Office:	Bossone 413F
Office Hours:	By appointment
Note:	I am accessible to discuss class-related issues at most times.

Audience

This course is intended for **graduate students** with interests in one or more of the following topics: computer architecture, computer networking, circuits and systems, VLSI.

Prerequisites

Knowledge of computer architecture (**ECEC621, minimum B-** grade) is required. In addition, knowledge in **at least one** of these two areas is required: 1) Hardware design (related courses **ECEC574/5/6 or ECEC671/2/3** or **ECEC661**), 2) Computer networking (**ECEC631**):

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Computer Architecture AND (Computer Networking OR VLSI)
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BS/MS degree students can substitute undergraduate equivalent of these courses. Only one of the prerequisite courses can be simultaneously registered with ECEC690 (i.e. at least one prerequisite course should have been successfully completed). Others are subject to instructor's approval.

Course Description

This is a graduate-level, introductory course in the field of *Networks-on-a-chip (NoC) design*. NoCs are the communication infrastructure between the many cores of a multi-processor system-on-a-chip (MPSoC), such as 1) a quad-core, eight-core, eighty-core and the futuristic 1000-core processors that target exa-scale computing or 2) multi-core systems that target high-performance mobile computing. Systematic understanding, design and analysis of NoCs will be covered. In particular, the focus will be on topics that include

1. Topology design,

2. Routing algorithms,

3. Router design,

4. Emerging NoC paradigms,

5. System-level performance metrics.

The course topics are mostly conceptual, as physical/industrial MPSoCs and NoCs are recently emerging trends with high complexity, and no educational prototypes are yet available. In this vein, in this course the following limitations exist:

1. No physical NoC design will be performed,
2. No design tools will be used,
3. No existing, industrial MPSoCs will be used,
4. No new design language will be introduced.

Instead, design technologies will be introduced conceptually and system-level performance will be measured with cycle-accurate NoC simulators such as `Booksim` and full-system simulators such as `gem5`.

Teaching Outcomes

The course objectives (i.e. teaching outcomes) include:

- To learn the basic concepts of NoC design by studying the topologies, router design and MPSoC styles,

- To learn sample routing algorithms on a NoC with deadlock and livelock avoidance,

- To understand the role of system-level design and performance metrics in choosing a NoC design,

- To observe the relationship between the requirements and implications of parallel computing/programming tasks on a many-core processor (e.g. with implications on shared/distributed memory system, local vs non-local communication patterns) and the design of a NoC within limited resources,

- To understand the relationship between semiconductor technology, computer architecture and computer networking in the design of the communication network for a MPSoC or a many-core design.

Textbook

Following is a list of suggested textbooks for this course, starting with the *required* textbook by Enright Jerger and Peh, which is available **online** through Drexel Library. The additional provide additional information that is not always NoC-specific but are quite useful in their broader schemes. If you are planning to get into this field seriously, you may also want to consider following periodical IEEE & ACM publications.

Required Textbook: N. Enright Jerger and L-S. Peh, *On-Chip Networks*, Synthesis Lectures on Computer Architecture, Morgan & Claypool, 2009, Electronic Resource, `http://www.morganclaypool.com/doi/abs/10.2200/S00209ED1V01Y200907CAC008`.

Additional Reading: 1. A Jantsch and H. Tenhunen, *Networks on Chip,* Kluwer Academic Publishers, 2003.
2. W. J. Dally, *Principles and Practices of Interconnection Networks*, Morgan Kaufmann, 2004.

Course Structure

Exam(s):	One (1) in-class examination.
Homework(s):	At least one (1) homework will be assigned.
Paper Review(s)	Two (2) paper reviews will be assigned.
Project(s):	One (1) project for teams of 2-to-4 will be assigned.

This is a graduate level class and the evaluation criteria is established accordingly. The evaluation process will encompass the monitoring of not the quality of individual work but also participation in group projects and lectures. The final grade will be calculated as follows:

Exam	$\rightarrow$	25%
Project(s)	$\rightarrow$	35%
Homework(s)	$\rightarrow$	15%
Paper Review(s)	$\rightarrow$	15%
Participation	$\rightarrow$	10%
Total		*100%*

The Academic Policies of Drexel University Office of the Provost dictates the scale of letter grades `http://www.drexel.edu/provost/policies/grades.asp`. Below are the percentages to be used in assignment of these grades:

Letter	Grade percentage
A+	100 – 97
A	96.9 – 93
A-	92.9 – 90
B+	89.9 – 87
B	86.9 – 83
B-	82.9 – 80
C+	79.9 – 77
C	76.9 – 73
C-	72.9 – 70
D+	69.9 – 67
D	66.9 – 63
F	Below 63

The instructor reserves the right to adjust the grade percentages (e.g. based on the distribution of grades) to accommodate non-standard (low or high) distributions.

Academic Policies

The academic policies defined by the Office of Provost are upheld for this course. The complete list of policies (academic and otherwise) are listed at `http://www.drexel.edu/policies/`. The students should particularly be aware of the following policies:

Academic Integrity	`http://www.drexel.edu/provost/policies/academic_dishonesty.asp`
	`http://www.drexel.edu/studentlife/judicial/honesty.html`
Course Drop Statement	`http://www.drexel.edu/provost/policies/course_drop.asp`
Disability Statement	`http://www.drexel.edu/oed/disabilityResources/`